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UTILITY PATENT APPLICATION TRANSMITTAL
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Docket No. 24705/99
Total Pages in this Submission

jc639 U.S. PTO 09/496421 02/02/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

jc584 U.S. PTO 09/496421 02/02/00

and invented by:

Ritsuko Iwasaki

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **21** pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets **6 (Figs. 1-8)**
   b. ☐ Informal Number of Sheets _____

4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☐ Certificate of Mailing
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Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	12	- 20 =	0	x	$18.00	$0.00
Indep. Claims	4	- 3 =	1	x	$78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)* Assignment Recordation						$40.00
					TOTAL FILING FEE	$808.00

☒ A check in the amount of **$808.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0481** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **February 2, 2000**

Sean M. McGinn, Esq.
Reg. No.: 34,386

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Customer No.: 21254

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APPLICATION FOR UNITED STATES LETTERS PATENT

APPLICANT: Ritsuko Iwasaki

FOR: SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

DOCKET NO.: 24705/99

SEMICONDUCTOR DEVICE

HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device, in particularly, to a layout of the semiconductor device which make it possible that electric characteristics of two transistors with the same structures as each other: so-called pair transistors, are manufactured with good manufacturing yield.

Description of the Related Art

A semiconductor device is manufactured by transferring a mask pattern in which a circuit configuration is laid out on a substrate to form a pattern of the configuration thereon. However, even if a mask pattern is prepared so as to satisfy circuit characteristics, an actual device manufactured on the substrate by using the pattern results in one without electric characteristics as expected when a dimensional difference due to parameter-related fluctuations in a manufacturing process arises. For example, even if masks with gate channel lengths L and gate channel widths W same as design values are prepared, actual devices formed with difference parameters from mask data when fluctuations of a manufacturing process or misalignment of masks for forming contacts are occurred.

Especially, in a case of a sense amplifier section or the like where a small current is employed, current amounts in halves of the circuit that are configured in symmetry with each other come into a state of off balance due to dimensional difference in actual layout, entails deterioration of electric characteristics and causes of defects.

Transistors (N1 and N2 of an A section of Fig. 8) that have symmetrical configurations with each other and which are required to have equal capabilities to each other have conventionally been manufactured with a drain region commonly used by two transistors as shown in Fig. 6, or alternatively with a source region commonly used by two transistors as shown in Fig. 7. Accordingly there has been arisen a problem that in a process step to manufacture such pair transistors, electric characteristics of the pair transistors become different from each other due to a dimensional difference caused by fluctuation of a manufacturing process.

This is a cause of a malfunction of a circuit, when the circuit has a symmetrical configuration as shown in Fig. 8 and halves of the circuit both operate under a difference of currents therebetween.

Further an actual width of a gate channel finally results in the sum of a mask design value (W) + a move-in of an insulating layer ΔW, relative to a mask design value. The move-in of the insulating layer ΔW causes in manufacture in which the insulating layer forming on a diffused region invades the diffused region in thermal diffusion. In an

actual design of a mask, dimensions of a mask pattern are determined in consideration of a move-in of an insulating layer ΔW in order to achieve high design precision. However the move-in ΔW arises in thermal diffusion is influenced by unexpected fluctuations of parameters in manufacture. Therefore it is difficult to avoid dimensional dispersion occurring beyond a design value ΔW from occurring.

As a difference of an actual width dispersion from a design tolerance ΔW is larger, a value of a channel width expected in proportion to the number of branch gates obtained division is not realized, and the number of branch gates or width of each branch gate is affected corresponding to a product of a move-in of an insulating layer ΔW * the number of branch gates. Therefore, if pair transistors in axial symmetry with each other are different in the number of branch gates from each other, it causes difference in actual channel width between the transistors completed, leading to a difference in performance therebetween as well.

Further, there arises a difference in actual gate width between an inner portion and an outer portion in a chip due to a difference in pattern packing density between an array section with a periodic pattern in which repeated gate patterns are densely packed in same intervals and a peripheral section with single patterns sparsely distributed as compared with the array section.

An additional difference in actual gate width between a densely packed section and a sparsely distributed section

in the same device occurs according to a degree of light straying-in under a pattern or a condition of light reflection in exposure.

While, in Japanese Patent Laid-Open No. 5-206245 and Japanese Patent Laid-Open No. 3-116726, dummy gates are employed in order to eliminate dimensional dispersion caused by a difference in pattern packing density according to regions where gates are arranged, the published documents have disclosed a technique on a circuit configured of single transistors, but not a technique on a circuit including pair transistors. Further, in Japanese Patent Laid-Open No. 62-173810, there has only been disclosed a transistor with a gate divided into a plurality of branch gates.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a semiconductor device having transistors with same electric characteristics.

It is another object of the present invention to provide a semiconductor device which can be manufactured while a dimensional dispersion in actual gate width according to light straying-in or light reflection in exposure is prevented from occurring and which makes it possible that transistors with same electric characteristics, such as pair transistors, are produced to high precision with good manufacturing yield.

It is another object of the present invention to provide pair transistors well suited for constructing a sense amplifier section employing a small current.

These and other objects of the present invention will be apparent to those of skill in the art from the appended claims when in light of the following specification and accompanying figures.

A semiconductor device according to the present invention includes a first transistor having a first gate put between a first source and a first drain; a second transistor arranged adjacent to the first transistor, the second transistor having a second gate put between a second source and a second drain, the second gate arranged parallel to the first gate; a first dummy gate arranged between the first drain and the second source and parallel to the first gate; a second dummy gate arranged adjacent to the first source and parallel to the first gate; and a third dummy gate arranged adjacent to the second drain and parallel to the first gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing an embodiment of a layout of a semiconductor device according to the present invention;

Fig. 2 is a plan view showing another embodiment of a layout of a semiconductor device according to the present invention;

Fig. 3 is a plan view showing a further embodiment of a layout of a semiconductor device according to the present invention;

Fig. 4 is tables showing states in which actual gate sizes are respectively different from design values thereof according to the number of gates;

Fig. 5 is plan views showing an example of an actual gate size corresponding to the number of gates;

Fig. 6 is a plan view showing a layout of a conventional semiconductor device;

Fig. 7 is a plan view showing another layout of a conventional semiconductor device; and

Fig. 8 is a diagram showing a circuit example for illustrating a problem in the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will be described in detail hereinafter with reference to the accompanying drawing:

Figs. 1 to 3 are views showing structures of a semiconductor device according to the present invention.

A first embodiment of the present invention is shown in Fig. 1.

In Fig. 1, there are shown pair transistors constituted of a first transistor 3A and a second transistor 3B. A dummy gate 3D2 is disposed between the transistors 3A and 3B, in

parallel to a gate 1 of a transistor 3A and a gate 11 of a transistor 3B, in a place equidistant from the gates 1 and 11. Dummy gates 3D1 and 3D3 are respectively disposed on the outsides of the transistors 3A and 3B. Any adjacent pair of the gates of the transistors 3A and 3B and the dummy gates have the same distance therebetween. Further, distances DIS3ct of electrode lead-outs of the dummy gates 3D1 to 3D3 are equal to distances of electrode lead-outs of the transistors 3A and 3B. Extension distances DIS3ext of the channel sections of the dummy gates 3D1 to 3D3 are the same as those of the pair transistors 3A and 3B. A source diffusion region 5 and a drain diffusion region 6 are formed in a semiconductor substrate (not shown) with an arrangement such that the gate 1 is sandwiched between the source and drain diffusion region 5, 6. The source and drain diffusion regions 5, 6 are surrounded by element isolation regions formed in the substrate.

The source electrode 15 is formed on the source diffusion region 5 to electrically connect with the source diffusion region 5 through contact 19 formed in an interlayer isolation layer between the source diffusion region 5 and the source electrode 15. The drain electrode 16 is formed on the drain diffusion region 6 to electrically connect with the drain diffusion region 6 through the contact 19 formed in the interlayer isolation layer.

Since the arrangement of the transistor 3A is substantially with that of the transistor 3B, the explanation

of source and drain diffusion region 1, 8 and source and drain electrodes 17, 18 are omitted.

The transistor 3A is, for example, a N channel transistor N1 and the transistor 3B is, for example, a N channel transistor N2, as shown in Fig.8. Therefore, the drain electrodes 16, 18 are connected in common to connect a GND potential through transistor N3.

With such dummy gates provided, the gate 1 of the transistor 3A and the gate 11 of the transistor 3B can be placed in exposure environments each with the same degree of light straying-in. Therefore, there arise no dimensional differences in manufacturing between the transistors 3A and 3B, enabling pair transistors each with a gate channel length L of the same order to be realized.

Furthermore, the transistors 3A and 3B each have a structure in which the source and drain regions formed on both sides of the gate are arranged in the same direction, which is different from conventional examples of FIGS. 6 and 7. In other words, the transistor 3B has the structure obtained by translating the transistor 3A while positional relations of the constituents therein are kept unchanged.

Reference marks are given to parameters associated with a semiconductor device with the structures as described above for clarity of description. In Fig. 1, distances from a channel of the transistor 3A to contacts are indicated by DIS31a and DIS32a; distances from a channel of the transistor 3B to contacts are indicated by DIS31b and DIS32b; amounts

of currents each flowing through the channel and contacts of each transistor are respectively indicated by I31a, I32a, I31b and I32b. Herein, distances DIS31a and DIS32a between the channel of the transistor 3A and the contacts on both sides thereof are equal and this relation applies to the transistor 3B.

The following is a description of a case where a registration error occurs when masks are stacked in the course of manufacturing of a transistor. When a mask is misplaced on another, contacts are formed at positions displaced in one direction. Therefore, as can be seen from Fig. 6 or 7, according to a conventional technique, pair transistors had respective different distances between gate channels and contacts on either of drain sides and source sides thereof. For example, when a misplacement of a mask occurs in a direction such that a relation DIS1 < DIS4 is established on the drain sides while a relation DIS3 < DIS2 is established on the source sides, there arises a difference between a current I1 that is dependent on a distance DIS1 and a current I4 that is dependent on a distance DIS4, which currents flow from the source to the drain, although a distance between the contacts of the source and drain of the transistors N1 is not changed and this also applies to the transistor N2. Hence, there arises a difference between currents flowing though the two transistors N1 and N2.

In the present invention, however, since the two transistors have structures in which DIS31a and DIS31b

thereof are equal to each other even when a mask pattern is formed with a deviation in one direction, therefore, a current I31a that is dependent on a distance DIS31a and which flows from the source to the drain of a transistor 3A is equal to a current I31b that is dependent on a distance DIS31b and which flows from the source to the drain of a transistor 3B. That is, there is no difference between the two transistors 3A and 3B in workings and a relation I31a + I32a = I31b + I32b is established and currents that respectively flow through the two transistors 3A and 3B can be made equal to each other.

Therefore, even if a mask pattern to form contacts is misplaced, no difference in characteristics between the transistors 3A and 3B occurs.

Fig. 2 shows a second embodiment of the present invention.

In Fig. 2, each of the gates of two transistors of Fig. 1 is forked into two branch gates and a structure is such that a channel of a transistor 4A is forked into two branch channels and distances DIS41a to DIS44a from the branch channels of the transistor 4A to contacts adjacent thereto are designed to be all the same as one another. Likewise, the transistor 4B has a two-way branched channel and a structure is such that distances DIS41b to DIS44b from the branch channels of the transistor 4B to contacts adjacent thereto are designed to be all the same as one another.

Dummy gates 4D1 and 4D2 of the same material and the same size as the gates 1 and 2 of the pair transistor 4A are arranged

on the left and right sides thereof. Likewise, dummy gates 4D2 and 4D3 of the same material and the same size as the gates 11 and 12 of the pair transistor 4B are arranged on the left and right sides thereof. Herein the dummy gate 4D2 commonly serves the pair transistors 4A and 4B.

In the structure, a distance between the branch gates of each of the transistors 4A and 4B; and a distance between each of the branched gates and the dummy gate adjacent thereto are all same: the branch gates of the transistors and the dummy gates are equidistantly arranged between any adjacent two thereof.

In addition, an electrode lead-out distance DIS4ct of the dummy gates 4D1 to 4D3 are the same as those of an electrode lead-out of the transistors 4A and 4B. Further, extension distances DIS4ext of the channel sections of the dummy gates 4D1 to 4D3 and those of the pair transistors 4A and 4B are all the same as one another.

With such dummy gates provided, the pair transistors each with two-way branched gates can be placed in exposure environments each with the same degree of light straying-in under a pattern. Hence, there arise no dimensional differences in manufacturing between the transistors 4A and 4B, thereby enabling pair transistors with the same characteristics as each other to be produced.

Furthermore, the transistors 4A and 4B each have a structure in which the source and drain regions formed on both sides of each of the gates are arranged in the same directions

like Fig. 1. Such a case where the gate of each of transistors is divided into two branch gates is nothing but a case of a structure in which the constituents of transistors are arranged in axial symmetry with each other. In Fig. 2, since a transistor has a two-way branched channel gate, the drain is disposed in a space between both end portions of the one source bent. Even if positional deviation of a mask pattern for forming contacts arises, source/drain currents of the two transistors are equal (I41a + I42a + I43a + I44a = I41b + I42b + I43b + I44b) with the result that there arises no difference in electric characteristics between the two transistors.

Fig. 3 shows a third embodiment of the present invention.

Each of the gates of two transistors in Fig. 1 is forked into three branch gates.

Since the transistors of this structure is essentially the same as those described in Fig. 1 in terms of workings, description thereof is omitted.

Transistors whose structures are in axial symmetry with each other have to have the respective same numbers of gate branches. Description will be made using Tables 1 to 6 of Fig. 4. A case is assumed where a move-in of an insulating layer $\Delta W = 0.2$ μm and corrected mask patterns ((a) in tables of Fig. 4) that are obtained by adding 0.2 μm to an expected value W of channel width are prepared.

If a width dispersion ΔW ((b) in tables of Fig. 4) arises in a diffusion process, an actual channel width W of each of the branch gates are shown as (c) in tables of Fig. 4 and sums

of channel widths W of all the actual branch gates are shown as (d) in tables of Fig. 4. It is understood, as shown in Tables 1 and 2, that if an estimation ΔW is obtained in thermal diffusion, expected results can be attained even when the number of branch gates is increased.

It is understood, however, that if there arises errors in estimation as compared with an expected ΔW of move-in of an insulating layer due to parameter-related fluctuations in manufacturing, expected results of mask patterns are harder to be actually attained as the number of branch gates increases as shown in Tables 3 to 6. This means that there is a limitation in realizing a mask design value W expected according to gate division. Values shown in the tables are obtained with the minimum size = 0.02 μm of a process currently employed set as the minimum size adopted in data preparation. Understanding is such that if it is desired that a capacitance of a diffused layer on the drain side is smaller, division into two or more branch gates is desired, while if it is desired that an actual width value W is closer to an expected width value W, the number of branch gates is necessary to be restricted to 2 to 3 branch gates.

As can be seen from the number of channel polysilicon stripes in arrangement and an actual channel length shown in Fig. 5, it is required that the gates of pair transistors are each divided into 2 to 3 branch gates and at least one dummy gate is provided, while such a requirement works for absorbing a change in ΔL in actual channel.

Since a semiconductor device according to the present invention has structures as described above, pair transistors with same electric characteristics can be attained even when a dimensional difference in patterning arises due to a cause in a manufacturing process.

While preferred embodiments of the present invention have been described, it is to be understood that the invention is to be defined by the appended claims when read in light of the specification and when accorded their full range of equivalent.

What is claimed is:

1. A semiconductor device comprising:

a first transistor having a first gate put between a first source and a first drain;

a second transistor arranged adjacent to said first transistor, said second transistor having a second gate put between a second source and a second drain, said second gate arranged parallel to said first gate;

a first dummy gate arranged between said first drains and said second source and parallel to said first gate;

a second dummy gate arranged adjacent to said first source and parallel to said first gate; and

a third dummy gate arranged adjacent to said second drain and parallel to said first gate.

2. The semiconductor device according to claim 1, wherein said first and second gate, said first, second and third dummy gate are the same as each other in shape.

3. The semiconductor device according to claim 1, wherein said first and second gate, said first, second and third dummy gate are evenly spaced.

4. The semiconductor device according to claim 1, wherein said first and second gate are respectively three-forked.

5. A semiconductor device comprising:

a first transistor having

a first source,

a first drain,

a first gate arranged between said first source and first drain,

a first contact hole formed on said first source and arranged at a first distance from said first gate, and

a second contact hole formed on said first drain and arranged at a second distance from said first gate, said second distance being the same with said first distance;

a second transistor arranged parallel to said first gate and having

a second source,

a second drain,

a second gate arranged between said second source and second drain,

a third contact hole formed on said second source and arranged at a third distance from said second gate, and

a fourth contact hole formed on said second drain and arranged at a fourth distance from said second gate, said fourth distance being the same with said third distance;

a first dummy gate set between said first drain and said second source and parallel to said first gate;

a second dummy gate set next to said first source and parallel to said first gate; and

a third dummy gate set next to said second drain and parallel to said first gate.

6. A semiconductor device including first and second transistors each having terminal commonly connected to a node; said device comprising:

a first gate electrode layer of said first transistor;

a first electrode layer of said first transistor coupled to a first contact hole;

a second electrode layer of said first transistor coupled to a second contact hole;

a second gate electrode layer of said second transistor;

a third electrode layer of said second transistor coupled to a third contact hole;

a fourth electrode layer of said second transistor coupled to fourth contact hole, said fourth electrode layer electrically coupled to said second electrode layer as said terminal;

wherein said first gate electrode layer, said first electrode layer, said second electrode layer, said second gate electrode layer, said third electrode layer, and said fourth electrode layer are arranged so that a first distance between said first contact hole and said first gate electrode layer keeps the same with a second distance between said third contact hole and said second gate electrode, and a third distance between said second contact hole and said first gate electrode layer keeps the same with a fourth distance between

said fourth contact hole and said second gate electrode layer while a mask for forming said first to fourth contact hole is misaligned.

7. The device as claimed in claim 6, wherein said first electrode layer, said first gate electrode layer, said second electrode layer, said third electrode layer, said second gate electrode layer, and said fourth electrode layer are arranged in that order in a line.

8. The device as claimed in claim 7, wherein said first electrode layer is a source of said first transistor, said second electrode layer is a drain of said first transistor, said third electrode layer is a source of said second transistor, and said fourth electrode layer is a drain of said second transistor.

9. The device as claimed in claim 8, said device further comprising:

a first dummy layer arranged between said second and third electrode layers;

a second dummy layer arranged so that said first electrode layer is sandwiched between said second dummy layer and said first gate electrode layer; and

a third dummy layer arranged so that said fourth electrode layer is sandwiched between said third dummy layer and said second gate electrode layer.

10. A semiconductor device comprising:

a first source diffusion region;

a first drain diffusion region;

a second source diffusion region;

a second drain diffusion region;

said first source diffusion region, said first drain diffusion region, said first source diffusion region, and said second drain diffusion region being arranged in that order on a line extending in a first direction, said first and second source diffusion regions and said first and second drain diffusion regions being surrounded by an element isolation region;

a first gate electrode formed between said first source and drain diffusion regions and extending in a second direction perpendicular to said first direction;

a second gate electrode formed between said second source and drain diffusion regions and extending in said second direction;

a first source electrode formed over said first source diffusion region and connected with said first source diffusion region through a first contact hole;

a first drain electrode formed over said first drain diffusion region and connected with said first drain diffusion region through a second contact hole;

a second source electrode formed over said second source diffusion region and connected with said second source diffusion region through a third contact hole;

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a second drain electrode formed over said second drain diffusion region and connected with said second drain diffusion region through a fourth contact hole.

11. The device as claimed in claim 10, said device further comprising:

a first dummy gate electrode arranged between said first drain and said second source electrodes on said element isolation region;

a second dummy gate electrode arranged on said element isolation region so that said first source electrode is sandwiched between said second dummy layer and said first gate electrode; and

a third dummy layer arranged on said element isolation region so that said second drain electrode is sandwiched between said third dummy layer and said second gate electrode.

12. The device as claimed in claim 11, wherein said first transistor includes said first source diffusion region, said first drain diffusion region, and said first gate electrode as one of N channel transistor pair and said second transistor includes said second source diffusion region, said second drain diffusion region, and said second gate electrode as the other of said N channel transistor pair electrically to connect said first drain electrode with said second drain electrode.

ABSTRACT

In a semiconductor device in which first and second transistors are configured so as to have the same electric characteristics as each other, a dummy gate is arranged between the first and second transistors in parallel to gates of the first and second transistors, and arrangement of source and drain regions formed on both sides of the gate of the first transistor, and arrangement of source and drain regions formed on both sides of the gate of the second transistor are the same as each other.

Fig.1

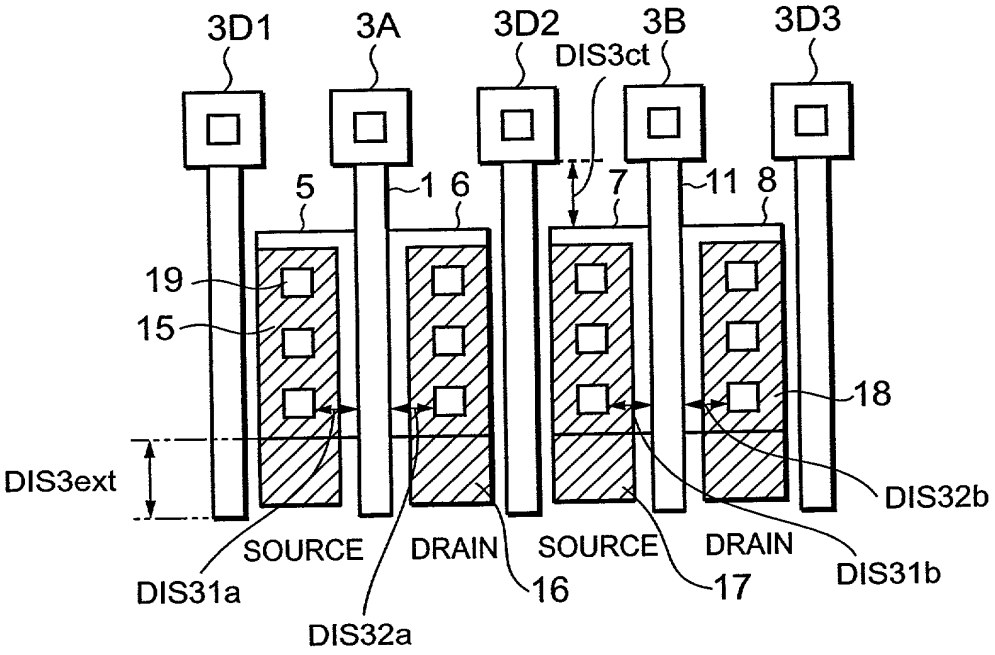

3D1
3A
3D2
3B
3D3
DIS3ct
5
1 6
7
11 8
19
15
18
DIS3ext
DIS32b
SOURCE
DRAIN
SOURCE
DRAIN
DIS31a
DIS31b
16
17
DIS32a

Fig.2

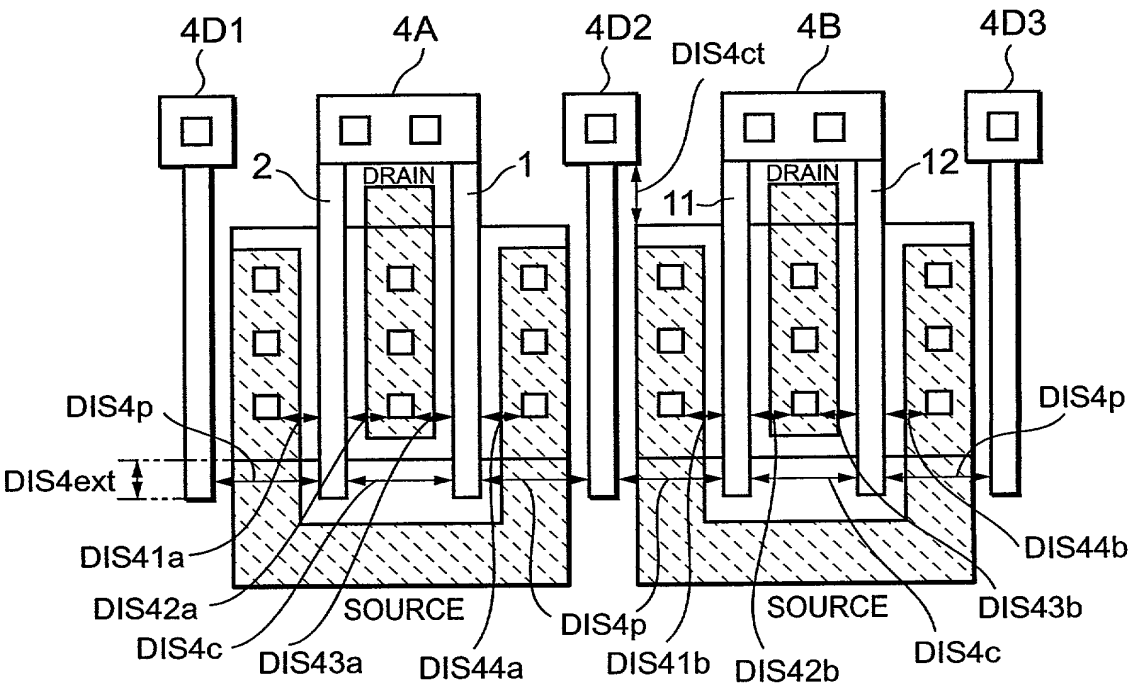

4D1
4A
4D2
DIS4ct
4B
4D3
2
DRAIN
1
11
DRAIN
12
DIS4p
DIS4ext
DIS41a
DIS42a
DIS4c
SOURCE
DIS43a
DIS44a
DIS4p
DIS41b
DIS42b
SOURCE
DIS4c
DIS43b
DIS44b
DIS4p

Fig.3

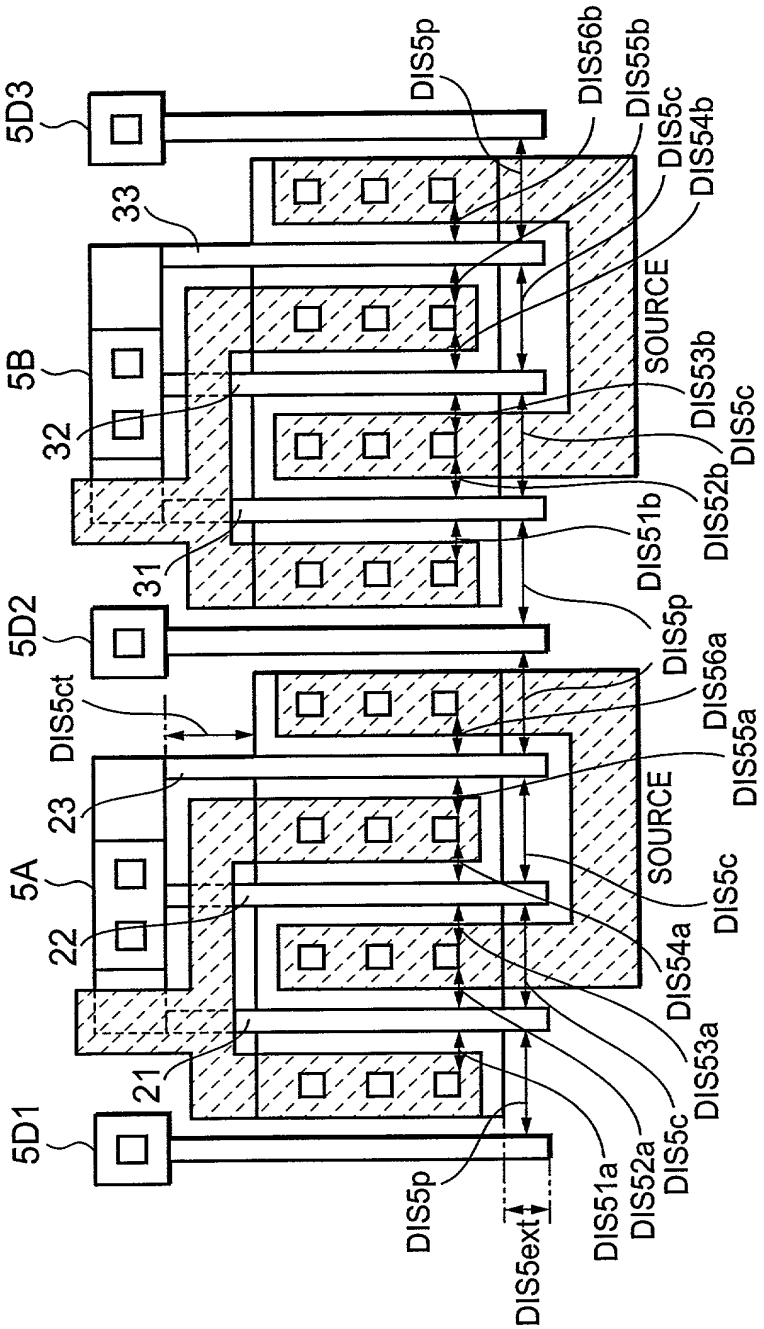

5D3
5B
5D2
5A
5D1
33
32
31
23
22
21
DIS5ct
DIS5p
DIS56b
DIS55b
DIS5c
DIS54b
SOURCE
DIS53b
DIS52b
DIS51b
DIS56a
DIS55a
DIS54a
DIS53a
DIS52a
DIS51a
DIS5ext

Fig.4

[TABLE 1] EXPECTED W=10 μm
DISPERSION(ΔW=0.2 μm)
<AS ESTIMATED>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	10.2	0.2	10	10
2	5.2	↓	5	10
3	3.54	↓	3.34	10.02
4	2.7	↓	2.5	10
5	2.2	↓	2	10
6	1.87	↓	1.67	10.02

[TABLE 2] EXPECTED W=15 μm
DISPERSION(ΔW=0.2 μm)
<AS ESTIMATED>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	15.2	0.2	15	15
2	7.7	↓	7.5	15
3	5.2	↓	5	15
4	3.96	↓	3.76	15.04
5	3.2	↓	3	15
6	2.7	↓	2.5	15

[TABLE 3] EXPECTED W=10 μm
DISPERSION(ΔW=0 μm)
<ESTIMATION ΔW-0.2μm>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	10.2	0	10.2	10.2
2	5.2	↓	5.2	10.4
3	3.54	↓	3.54	10.64
4	2.7	↓	2.7	10.8
5	2.2	↓	2.2	11
6	1.87	↓	1.87	11.22

[TABLE 4] EXPECTED W=15 μm
DISPERSION(ΔW=0 μm)
<ESTIMATION ΔW-0.2μm>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	15.2	0	15.2	15.2
2	7.7	↓	7.7	15.4
3	5.2	↓	5.2	15.6
4	3.96	↓	3.96	15.84
5	3.2	↓	3.2	16
6	2.7	↓	2.7	16.2

[TABLE 5] EXPECTED W=10 μm
DISPERSION(ΔW=0.4 μm)
<ESTIMATION ΔW+0.2μm>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	10.2	0.4	9.8	9.8
2	5.2	↓	4.8	9.6
3	3.54	↓	3.14	9.42
4	2.7	↓	2.3	9.2
5	2.2	↓	1.8	9
6	1.87	↓	1.47	8.82

[TABLE 6] EXPECTED W=15 μm
DISPERSION(ΔW=0.4 μm)
<ESTIMATION ΔW+0.2μm>

NUMBER OF GATES	(a) MASK-DESIGN VALUE	(b) DIS-PERSION (ΔW)	(c) ACTUAL GATE WIDTH	(d) SUM OF ACTUAL GATE WIDTHS
1	15.2	0.4	14.8	14.8
2	7.7	↓	7.3	14.6
3	5.2	↓	4.8	14.4
4	3.96	↓	3.56	14.24
5	3.2	↓	2.8	14
6	2.7	↓	2.3	13.8

Fig.5

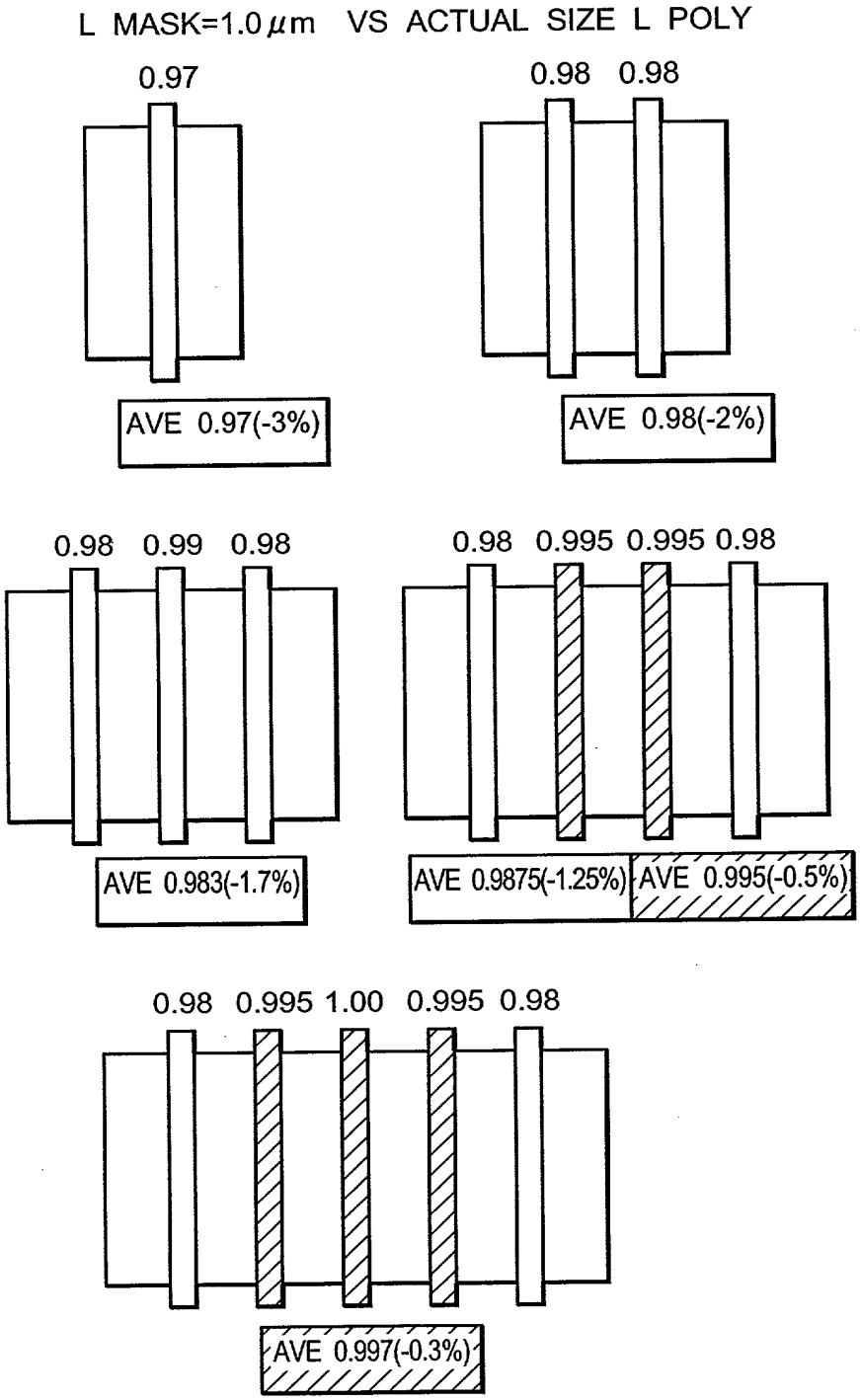

L MASK=1.0μm VS ACTUAL SIZE L POLY
0.97
AVE 0.97(-3%)
0.98 0.98
AVE 0.98(-2%)
0.98 0.99 0.98
AVE 0.983(-1.7%)
0.98 0.995 0.995 0.98
AVE 0.9875(-1.25%)
AVE 0.995(-0.5%)
0.98 0.995 1.00 0.995 0.98
AVE 0.997(-0.3%)

Fig.6

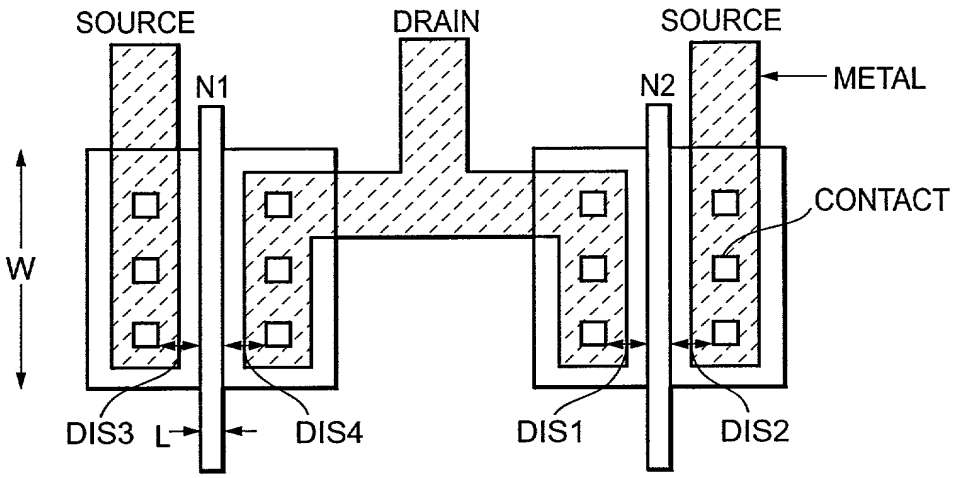


Fig.7

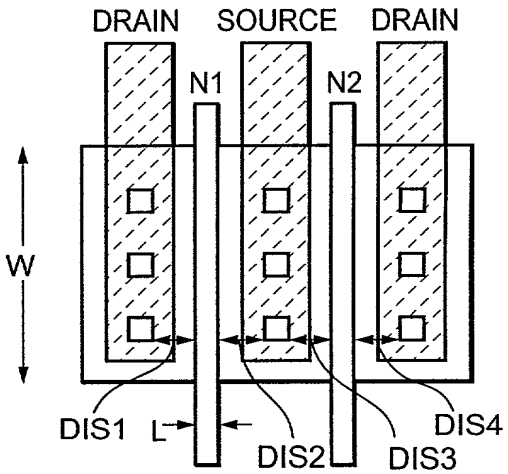
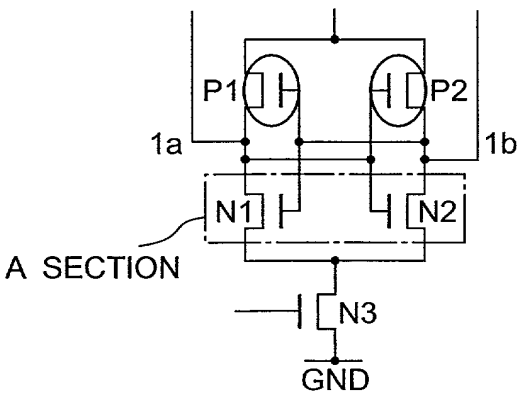


Fig.8



Application for United States Patent

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

the specification of which:

(check one)

☒ is attached hereto

☐ was filed on _____, as Application Serial No. _____ and was amended on _____. (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56*

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			priority claimed	
24705/1999	Japan	2/2/1999	X	
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
(Number)	(Country)	(Day/Month/Year Filed)	yes	no

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

Power of Attorney: As a named inventor, I hereby appoint Sean M. McGinn, Reg. 34,386, and Frederick W. Gibb, III, Reg. No. 37,629 as attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. All correspondence should be directed to **McGinn & Gibb, P.C., 1701 Clarendon Boulevard, Suite 100, Arlington, Virginia 22209**. Telephone calls should be directed to McGinn & Gibb, P.C. at **(703) 294-6699**.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful

false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Ritsuko Iwasaki Date 1/27/2000

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Full Name of Second Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

Full Name of Third Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

Full Name of Fourth Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

(An additional sheet(s) is/are attached hereto if the present invention includes more than four inventors.)

*Title 37, Code of Federal Regulations, § 1.56:

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith toward the Patent and Trademark Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and (1) it establishes , by itself or in combination with other information, a prima facie case of unpatentability; or (2) it refutes, or is inconsistent with, a position the applicant takes in: (i) opposing an argument of unpatentability relied on by the Office, or (ii) asserting an argument of patentability.